Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-8. (Canceled)

9. (Currently Amended) A method of generating a combined code comprising:

a) combining a plurality of codes each having a length shorter than the combined code, the plurality of codes including at least three codes having lengths m, n, and p, where m, n, and p, are mutually prime, wherein the combined code has a length of $3 \bullet n \bullet m \bullet p$; and

b) outputting the combined code, wherein the plurality of codes can be detected from the combined code, and the phases of the combined code can be detected from the plurality codes.

11-16. (Canceled)

17. (Previously Presented) A method of generating a code, comprising:

a) generating a symbol of a first code of length n symbols;

b) generating a symbol of a second code of length m symbols, where m is greater than n;

c) generating a third code by outputting the symbol of the first code followed by the symbol of the second code; and

d) repeating a) through c) at least $2 \bullet n \bullet m$ times.

18. (Original) The method of generating a code according to claim 17, wherein in a) the symbols of the first code are generated in order, modulo n, and in b) the symbols of the second code are generated in order, modulo m.

19. (Previously Presented) A method of generating a code, comprising:

a) generating a symbol of a first code of length n symbols;

b) generating a symbol of a second code of length m symbols, where m is greater than n;

c) generating a third code by outputting the symbol of the first code followed by the symbol of the second code;

d) repeating a) through c) a predetermined number of times less than n•m times; and

e) outputting an output signal having a predetermined number of symbols less than 2•n•m symbols.

20. (Previously Presented) The method of generating a code according to claim 19, wherein each symbol is comprised of chips representing a binary value.

21-26. (Canceled)

27. (Previously Presented) A transmitter, comprising:

a controller outputting first, second and third control signals based on a count;

a first code generator generating a first code of n symbols in response to the first control signal;

a second code generator generating a second code of m symbols in response to the second control signal, where m is greater than n; and

a multiplexer coupled to the controller and the first and second code generators, for interleaving symbols of the first code with the symbols of the second code, wherein the controller outputs a signal to the multiplexer to output only selected portions of one or more of the first and second codes, so that the interleaved code has a length less than 2•n•m symbols.

28-32. (Canceled)

33. (Previously Presented) A transmission signal having a sequence of symbols, the sequence comprising symbols of a first code of n symbols interleaved with symbols of a second

code of m symbols, wherein the first code repeats modulo n and the second code repeats modulo m, and the sequence repeats modulo 2•n•m.

34. (Previously Presented) The transmission signal of claim 33, wherein each symbol is comprised of chips that each represents a binary value.

35. (Currently Amended) A method of determining the phase of a transmitted code generated by combining at least a first code and a second code, comprising:

detecting a phase of the first code;

detecting a phase of the second code; and

determining the phase of the transmitted code from the phases of the first and second codes using the Chinese Remainder Theorem, wherein the transmitted code is generated by interleaving the first and second codes.

36. (Canceled)

37. (Previously Presented) A code generating apparatus for generating an output code of a predetermined length, comprising:

a first code generator configured to generate a first code of n symbols;

a second code generator configured to generate a second code of m symbols, wherein values of m and n permit generation of a code that repeats modulo 2•n•m symbols by interleaving symbols of the first and second codes, and 2•n•m symbols exceeds the predetermined length; and

a combiner configured to interleave symbols of the first and second codes to generated the output code having a number of symbols corresponding to the predetermined length, wherein the number of symbols is less than 2•n•m.

38. (Previously Presented) The apparatus of claim 37, wherein the combiner truncates symbols relative to a code of 2•n•m symbols to generate the output code.

39. (Previously Presented) The apparatus of claim 37, wherein the combiner omits symbols of a code of 2•n•m symbols to generate the output code.

40. (Previously Presented) A method of generating an output code of a predetermined length, comprising:

generating a first code of n symbols;

generating a second code of m symbols, wherein values of m and n permit generation of a code that repeats modulo 2•n•m symbols by interleaving symbols of the first and second codes, and 2•n•m symbols exceeds the predetermined length; and

interleaving symbols of the first and second codes to generated the output code having a number of symbols corresponding to the predetermined length, wherein the number of symbols is less than 2•n•m.

41. (Currently Amended) The method of claim 40 ~~37~~, wherein symbols are truncated from a code of 2•n•m symbols to generate the output code.

42. (Currently Amended) The ~~apparatus~~ method of claim 40 ~~37~~, wherein symbols are omitted from a code of 2•n•m symbols to generate the output code.